1.FEATURES

- Band: 30MHz to 5000MHz
- Supports TDD and FDD operation
- Tunable channel bandwidth: 1.4MHz to 20 MHz
- Dual receiver: 6 differential or 12 single-ended inputs
- Superior receiver sensitivity with a noise figure of 4 dB
- RX gain control:
  - Real-time monitoring and control signals for manual gain
  - Independent automatic gain control
- Single transmitter: 2 differential output
- TX power range: 48dB
- TX EVM: ≤ -40 dB
- TX noise: ≤ -157 dBm/Hz noise floor
- TX monitor: ≥ 40 dB dynamic range with 1 dB accuracy
- Integrated fractional-N synthesizer

2.APPLICATIONS

- General-purpose radio systems
- Femtocell/Picocell/Microcell base stations
- Multifunctional smart terminals
- Point-to-point communication systems

3.GENERAL DESCRIPTION

The GC0851 is a high-performance, highly integrated ultra-wideband SDR transceiver that can be widely used in almost all modern digital wireless communication systems. The GC0851 LO operates from 30MHz to 5000MHz. Channel bandwidth from 1.4MHz to 20MHz are supported.

The GC0851 built-in programmable analog filter supports a minimum 0.7MHz bandwidth and a maximum 10MHz bandwidth for TX/RX analog low-pass filter. The mixer and phase-locked loop are also integrated inside the chip, and the transmit path includes a driver amplifier.

The GC0851 applies direct conversion architecture to achieve high modulation accuracy and ultra-low noise. The chip supports image suppression calibration, LO leakage calibration, transmit power monitoring, spurious suppression, and receive channel gain calibration. Register read and write adopts standard four-wire SPI. The GC0851 is packaged in a 4.5 mm x 5 mm, 82-ball chip scale package ball grid array (CSP_BGA).

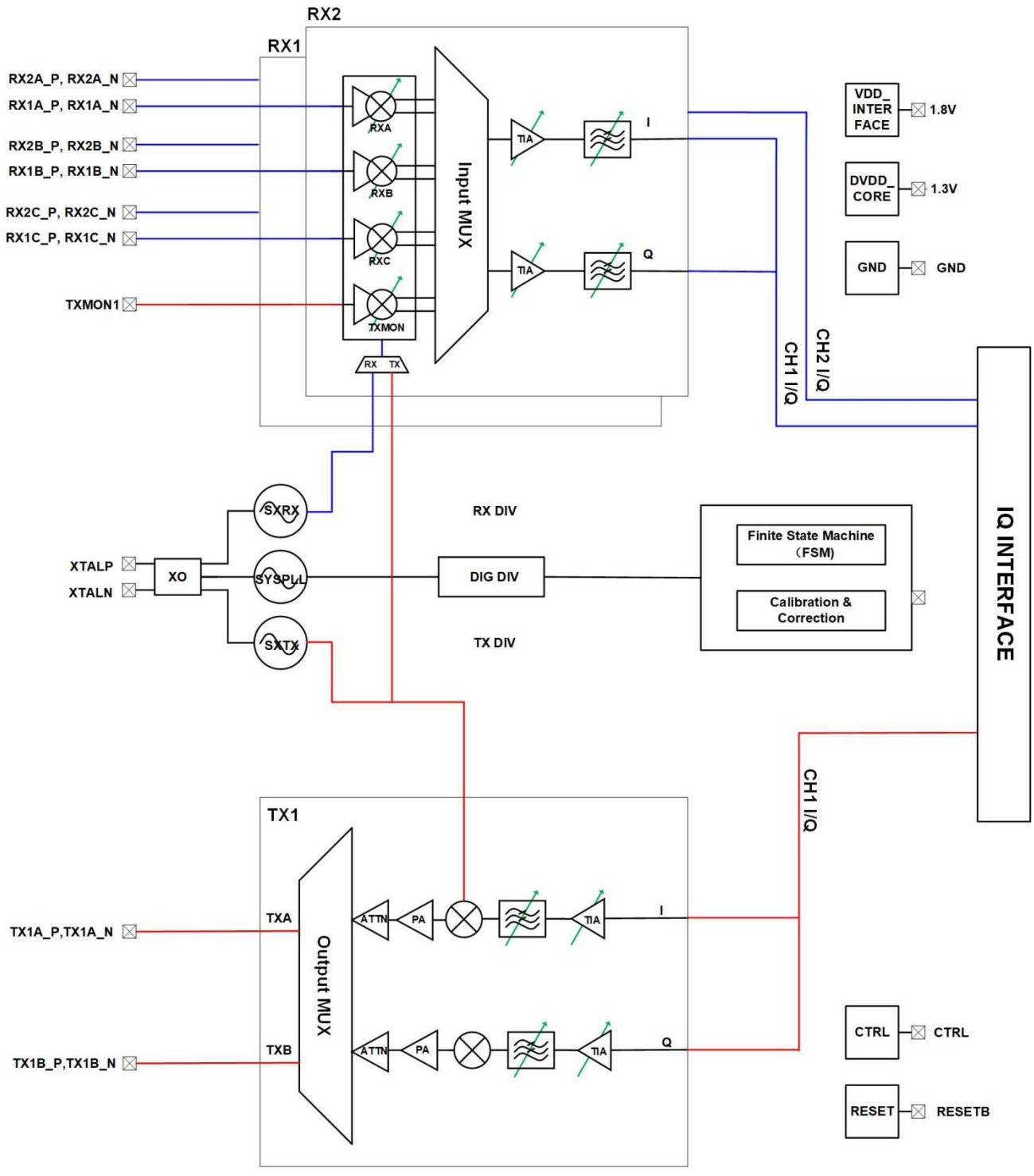

Figure 1 System diagram of GC0851

CONTENTS

4. Product specifications

4.1 Absolute maximum ratings

Parameter	Rating
VDDx to VSSx	-0.3V~ +1.5V
VDD_INTERFACE to VSSx	-0.3V~ +3.3V
Logical inputs and outputs to VSSx	-0.3V to VDD_INTERFACE+0.3V
Input current to any pin except power supply pins	±10mA
RF inputs (peak power)	2.5 dBm
Maximum junction temperature (TJMAX)	110 ℃
Operating temperature range	- 40 ~ +85 ℃
Storage temperature range	- 65 ~ +150 ℃

Table 1

Note: Exceeding the absolute maximum rating above may result in permanent damage to the device. This is the maximum rating only and cannot be used to infer the normal operation of the device under these conditions or any other conditions beyond the specifications indicated in the operating section of this Technical specification. Prolonged operation under absolute maximum rating conditions will affect the reliability of the device.

4.2 Recommended working conditions

Parameters	Recommended Values
VDDx	+1.3V (the practical acceptable range is between 1.3V-1.5V)
VDD_INTERFACE	+ 1.8 V
Working ambient temperature	- 40 ~ +85 ℃

Table 2

4.3 Thermal resistance

Package Type	Θ_{JA}	Θ_{JB}	Θ_{JC}	Units
82-Ball (CSP-BGA)	39.4	20.9	22.9	℃/W

Table 3

4.4 Reflux temperature curve

The GC0851 reflux temperature curve is based on the JEDEC JESD20 device standard. The maximum reflux temperature is +260℃.

4.5 ESD caution

ESD(electrostatic discharge) sensitive devices

Live devices and circuit boards may be powered down without being noticed. Although this product has a patented or proprietary protection circuit, the device may be damaged when exposed to high energy ESD. Therefore, appropriate ESD protection measures should be taken to avoid degradation of device performance or loss of function.

Model	Pins	Minimum ESD Rating	Unit
ESD Charge Device Model(CDM), ANSI/ESDA/JEDEC JS-002-2022	All pins	±500	V
ESD Human Body Model(HBM), ESDA/JEDEC JS-001-2017	All pins	±2000	V
LATCH-UP TEST(LU), JESD78F.02-2023	All pins	±200	mA

Table 4

5. Package and pin function descriptions

5.1 Outline dimensions (in millimeters)

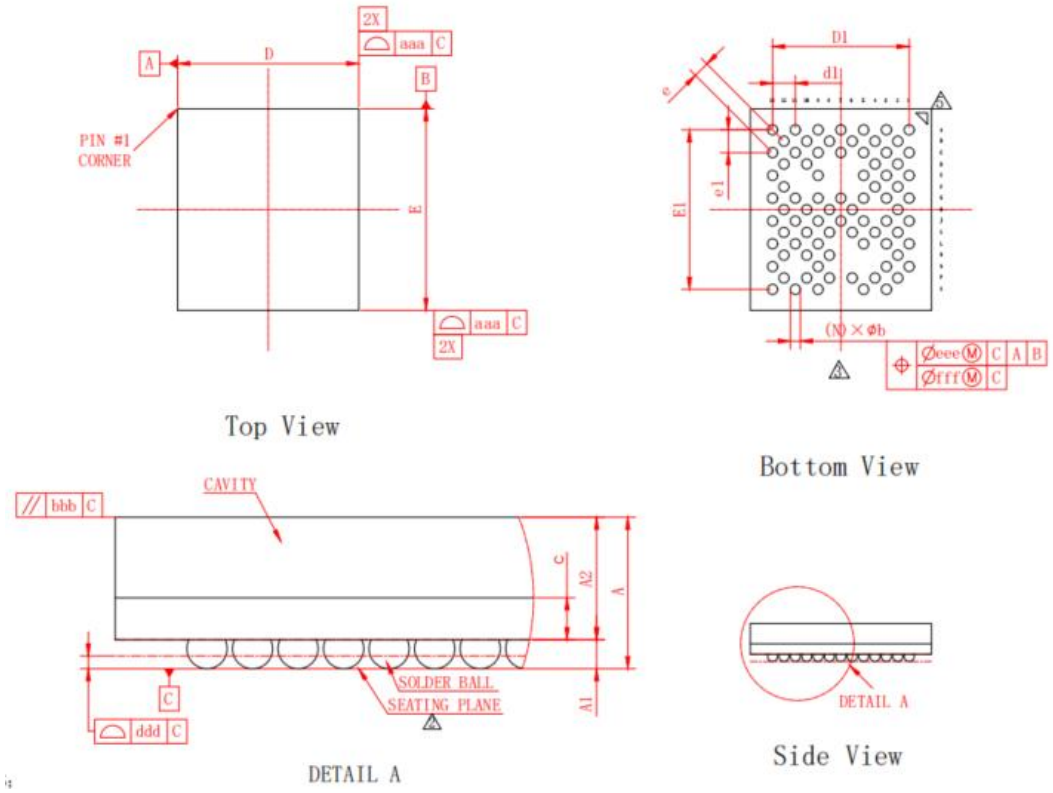

Figure 2

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.840	0.940	1.040	0.033	0.037	0.041
A1	0.130	0.180	0.230	0.005	0.007	0.009
A2	0.700	0.760	0.820	0.028	0.030	0.032
c	0.230	0.260	0.290	0.009	0.010	0.011
D	4.400	4.500	4.600	0.173	0.177	0.181
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	---	3.396	---	---	0.134	---
E1	---	3.962	---	---	0.156	---
d1	---	0.566	---	---	0.022	---
e	---	0.400	---	---	0.016	---
e1	---	0.566	---	---	0.022	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	82			82		
MD/ME	13/15			13/15		

Figure 3

5.2 Pin function descriptions

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	TX MON1		RX1AP		RX1BP		RX1CP		RX2CP		RX2BP		RX2AP
B		RX1AN		RX1BN		RX1CN		RX2CN		RX2BN		RX2AN	
C	VDD1P3 TX1		VSSA		VDD1P3 RX		VSSA		VSSA		VSSA		VSSA
D		AVDD13 ADDA1		PAD RX1IFQN						VSSA		VSSA	
E	TX1AP		VSSA		PAD RX1IFQP				VSSA				AVDD13 ADDA2
F		TX1AN		PAD RX1IFIP								VDD1P3 TX2	
G	TX1BP		VSSA		PAD RX1IFIN		PAD RX2IFQN		VSSA		CTRLIN1		VDD1P3 RF
H		TX1BN				VSSA		PAD RX2IFQP		VSSA		CTRLIN0	
J	VSSA		VSSA		VSSA		PAD RX2IFIP		VSSA		CTRLOUT7		VSSA
K		XTALP		VSSA		VSSA		PAD RX2IFIN		VSSA		CTRLIN3	
L	XTALN		VSSA		VSSA				VSSA		CTRLOUT3		TESTENABLE
M		AVDD13 LFCK						RESETB		ENABLE		CTRLIN2	
N	RBIAS		VSSA						TXNRX				VDD1P3 DIG
P		TX1EXT DAC IIOUTB		TX1EXT DAC QIOUTB		VSSA		SPICLK		SPIENB		VDD INTERFACE	
R			TX1EXT DAC IIOUT		TX1EXT DAC QIOUT				SPIDI		SPIDO		VDDGPO

Figure 4

Pin Number	Type	Pin name	Description
A1	I	TX_MON1	Transmit channel 1 power monitoring input.Tie unused pins to ground with a capacitor
A3,B2	I	RX1A_N, RX1A_P	Receive channel 1 Differential input A. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A5,B4	I	RX1B_P, RX1B_N	Receive channel 1 Differential input B. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A7,B6	I	RX1C_P, RX1C_N	Receive channel 1 Differential input C. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A9,B8	I	RX2C_N, RX2C_P	Receive channel 1 Differential input C. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A11,B10	I	RX2B_P, RX2B_N	Receive channel 1 Differential input B. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A13,B12	I	RX2A_P, RX2A_N	Receive channel 1 Differential input A. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
C1	I	VDD1P3_TX1	TX1 1.3V power supply input
C3,C7,C9,C11,C13,D10,D12,E3,E9,G3,G9,H10,H6,J1,J3,J5,J9,J13,K4,K6,K10,L3,L5,L9,N3,P6	I	VSSA	Analog ground
C5	I	VDD1P3_RX	Receive 1.3V power supply input
D2	I	AVDD13_ADDA1	1.3V power supply input
D4,E5	O	PAD_RX1IFQN PAD_RX1IFQP	Receive channel 1 IF difference Q output. Do not connect if not used
E1,F2	O	TX1A_P, TX1A_N	Transmit channel 1 Differential output A. If unused, do not connect these pins
E13	I	AVDD13_ADDA2	1.3V power supply input
F4,G5	O	PAD_RX1IFIN PAD_RX1IFIP	Receive channel 1 IF difference I output. Do not connect if not used
F12	I	VDD1P3_TX2	TX2 1.3V power supply input
G1,H2	O	TX1B_P, TX1B_N	Transmit channel 1 Differential output B. If unused, do not connect these pins
G7,H8	O	PAD_RX2IFQN PAD_RX2IFQP	Receive channel 2 IF difference Q output. Do not connect if not used
G11,H12,K12,M12	I	CTRL_IN1,CTRL_IN0,CTRL_IN3,CTRL_IN2	Control input. Manual RX gain and TX attenuation control
G13	I	VDD1P3_RF	RF 1.3V power supply input
J7,K8	O	PAD_RX2IFIN PAD_RX2IFIP	Receive channel 2 IF difference I output. Do not connect if not used
J11,L11	O	CTRL_OUT7,CTRL_OUT3	Control Outputs. These pins are multipurpose outputs that have programmable functionality
L1,K2	I	XTALP, XTALN	Reference Frequency Crystal Connections. When a crystal is used, connect it between these two pins. When an external clock source is used, connect it to XTALN and leave XTALP unconnected
K13	O	TEST_ENABLE	
M2	I	AVDD13_LFCK	SYSPLL/XO 1.3 V power supply input
M8	I	RESETB	Asynchronous reset. Logic low resets the device
M10	O	ENABLE	Control input. This pin moves the device through various operational states
N1	I	RBIAS	Bias Input Reference. Connect this pin through a 14.3

			kΩ (1% tolerance) resistor to ground
N9	I	TXNRX	Enable state machine control signals. This pin controls the data port bus direction. Logic low selects the RX direction and logic high selects the TX direction
N13	I	VDD1P3_DIG	1.3V digital power supply input
P2,R3	O	TX1_EXT_DAC_I_Iout TX1_EXT_DAC_I_OutB	Transmit channel1 analog I differential output, tie to ground when not used
P4,R5	O	TX1_EXT_DAC_Q_Iout, TX1_EXT_DAC_Q_IOutB	Transmit channel1 analog Q differential output, tie to ground when not used
P8	I	SPI_CLK	SPI clock input
R9	I	SPI_DI	SPI serial data input
P10	I	SPI_ENB	SPI Enable input. Set this pin to logic low to enable the SPI bus
R11	O	SPI_DO	SPI serial data output
P12	I	VDD_INTERFACE	1.8 V to 3.3 V Supply for Digital I/O Pins
R13	I	VDD_GPO	NC

Table 5 Pin descriptions

6. Specifications

6.1 Receiver

Electrical characteristics at VDD_INTERFACE = 1.8V, and all other VDDx pins = 1.3V, unless otherwise noted.

TA=25℃:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Min analog gain			8		dB	
Max analog gain		48	50	52	dB	50 dB@2.4GHz
Analog gain step			1		dB	
BB filter order			4			
Receiver 773MHz						
Noise figure	NF		3.5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-3		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point	IIP2		52		dBm	Maximum RX gain,20M BW,Single end N
			55		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			2.5		%	26 MHz reference clock; LTE20M, 64QAM
RX BB filter selectivity BW 1.4 MHz:			5		dBc	800kHz
			45		dBc	2.8MHz
			60		dBc	4.2MHz
			70		dBc	5.6MHz
RX BB filter selectivity BW 3 MHz:			5		dBc	1.5MHz
			35		dBc	3.5MHz
			45		dBc	5MHz
			65		dBc	15MHz
			70		dBc	>80MHz
RX BB filter selectivity BW 5 MHz			4		dBc	2.5MHz
			10		dBc	3,5MHz
			25		dBc	5MHz
			55		dBc	15MHz
			55		dBc	>80MHz
RX BB filter selectivity BW 10MHz			5		dBc	5.3MHz
			15		dBc	7.5MHz
			35		dBc	12.5MHz
			45		dBc	20MHz
			55		dBc	>80MHz
RX BB filter selectivity BW 15MHz			4.5		dBc	7.6MHz
			20		dBc	15MHz
			30		dBc	20MHz
			50		dBc	>80MHz
RX BB filter			6		dBc	10.1MHz

selectivity BW 20MHz			20		dBc	15MHz
			35		dBc	22.5MHz
Input S11			50		dBc	>80MHz
Receiver 2150MHz						
Noise figure	NF		4.2		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-3		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point	IIP2		49		dBm	Maximum RX gain,20M BW,Single end N
			50		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			2.5		%	26 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	
Receiver 2665MHz						
Noise figure	NF		5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-3		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			2.5		%	26 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	
Receiver 3500MHz						
Noise figure	NF		5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-4		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3.5		%	26 MHz reference clock; LTE20M, 64QAM
Input S11			-10		dB	

Table 6 Receiver specifications(Normal temp)

TA=85℃:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Min analog gain			8		dB	
Max analog gain		48	50	52	dB	50 dB@2.4GHz
Analog gain step			1		dB	
BB filter order			4			
Receiver 773MHz						
Noise figure	NF		3.5		dB	Maximum RX gain
Third-Order Input Intermodulation	IIP3		-4		dBm	Maximum RX gain

Intercept Point						
Second order Input Intermodulation Intercept Point	IIP2		48		dBm	Maximum RX gain,20M BW,Single end N
			50		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 2150MHz						
Noise figure	NF		5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-4		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point	IIP2		48		dBm	Maximum RX gain,20M BW,Single end N
			52		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3.5		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 2665MHz						
Noise figure	NF		5.5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-4		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3.5		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 3500MHz						
Noise figure	NF		6.5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-5		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			4		%	26 MHz reference clock; LTE20M, 64QAM

Table 7 Receiver specifications(High temp)

TA=-40℃:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Min analog gain			8		dB	
Max analog gain		48	50	52	dB	50 dB@2.4GHz
Analog gain step			1		dB	
BB filter order			4			
Receiver 773MHz						
Noise figure	NF		3		dB	Maximum RX gain
Third-Order Input Intermodulation	IIP3		-4		dBm	Maximum RX gain

Intercept Point						
Second order Input Intermodulation Intercept Point	IIP2		52		dBm	Maximum RX gain,20M BW,Single end N
			55		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			2.5		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 2150MHz						
Noise figure	NF		4		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-3		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point	IIP2		50		dBm	Maximum RX gain,20M BW,Single end N
			53		dBm	Maximum RX gain,10M BW,Single end N
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 2665MHz						
Noise figure	NF		4.5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-3		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3		%	26 MHz reference clock; LTE20M, 64QAM
Receiver 3500MHz						
Noise figure	NF		6.5		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-5		dBm	Maximum RX gain
Image suppression	IMRR		30		dBc	Before cal
DC rejection	DC			10	mV	
Modulation accuracy (EVM)			3		%	26 MHz reference clock; LTE20M, 64QAM

Table 8 Receiver specifications(Low temp)

6.2 Transmitter

Electrical characteristics at VDD_INTERFACE = 1.8V, and all other VDDx pins = 1.3V, Single channel IQ Signal Vpp=360mV,unless otherwise noted.
T_A= 25°C:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Analog power control range		46	48	50	dB	48 dB@2.4GHz
Analog power control step			1		dB	
TX Monitor (TX_MON1)						
Dynamic range			41		dB	
Accuracy			1		dB	
Transmitter 718MHz						
Output S22			- 10		dB	
Maximum output power			-3		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			- 48		dBc	20M offset
Carrier leakage			- 55		dBc	40M offset
Image suppression			50		dBc	Before cal
CIM3			58		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			- 157		dBm/Hz	BW <=10M，30M offset
			- 157		dBm/Hz	BW <=15M，45M offset
			- 157		dBm/Hz	BW <=20M，55M offset
Transmitter 1960MHz						
Output S22			- 10		dB	
Maximum output power			- 3.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1.2		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-48		dBc	20M offset
Carrier leakage			- 55		dBc	40M offset
Image suppression			55		dBc	Before cal
CIM3			58		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 2665MHz						
Output S22			- 10		dB	
Maximum output			- 3.5		dBm	Modulation LTE 20M 64QAM

power						
Minimum output power			-51.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1.5		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-48		dBc	20M offset
Carrier leakage			-52		dBc	40M offset
Image suppression			45		dBc	Before cal
CIM3			66		dBc	
CIM5			79		dBc	
CIM7			79		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 3500MHz						
Output S22			- 10		dB	
Maximum output power			- 4		dBm	Modulation LTE 20M 64QAM
Minimum output power			-52		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			2		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-48		dBc	20M offset
Carrier leakage			-55		dBc	40M offset
Image suppression			40		dBc	Before cal
CIM3			72		dBc	
CIM5			79		dBc	
CIM7			79		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset

Table 9 Transmitter specifications

TA = 85°C:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Analog power control range		46	48	50	dB	48 dB@2.4GHz
Analog power control step			1		dB	
TX Monitor (TX_MON1)						
Dynamic range			41		dB	
Accuracy			1		dB	
Transmitter 718MHz						
Maximum output power			-3.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1		%	26 MHz reference clock; LTE20M, 64QAM
ACLR			- 46		dBc	20M offset

			- 55		dBc	40M offset
Image suppression			50		dBc	Before cal
CIM3			57		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			- 157		dBm/Hz	BW <=10M，30M offset
			- 157		dBm/Hz	BW <=15M，45M offset
			- 157		dBm/Hz	BW <=20M，55M offset
Transmitter 1960MHz						
Maximum output power			- 4		dBm	Modulation LTE 20M 64QAM
Minimum output power			-52		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1.5		%	26 MHz reference clock; LTE20M, 64QAM
ACLR			-48		dBc	20M offset
			- 55		dBc	40M offset
Image suppression			40		dBc	Before cal
CIM3			59		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 2665MHz						
Maximum output power			- 4		dBm	Modulation LTE 20M 64QAM
Minimum output power			-52		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			2		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-48		dBc	20M offset
Carrier leakage			-55		dBc	40M offset
Image suppression			45		dBc	Before cal
CIM3			70		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 3500MHz						
Maximum output power			- 4.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-52.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			2		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-45		dBc	20M offset
Carrier leakage			-55		dBc	40M offset
Image suppression			40		dBc	Before cal
CIM3			69		dBc	

CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset

Table 10 Transmitter specifications(High Temp)

TA = -40°C:

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency		30		5000	MHz	
Channel bandwidth		1.4		20	MHz	
Analog power control range		46	48	50	dB	48 dB@2.4GHz
Analog power control step			1		dB	
TX Monitor (TX_MON1)						
Dynamic range			41		dB	
Accuracy			1		dB	
Transmitter 718MHz						
Maximum output power			-2.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-50.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			- 45		dBc	20M offset
Carrier leakage			- 55		dBc	40M offset
Image suppression			40		dBc	Before cal
CIM3			58		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			- 157		dBm/Hz	BW <=10M，30M offset
			- 157		dBm/Hz	BW <=15M，45M offset
			- 157		dBm/Hz	BW <=20M，55M offset
Transmitter 1960MHz						
Maximum output power			- 3		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1		%	26 MHz reference clock; LTE20M, 64QAM
Carrier leakage			-48		dBc	20M offset
Carrier leakage			- 55		dBc	40M offset
Image suppression			40		dBc	Before cal
CIM3			59		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 2665MHz						

Maximum output power			- 3.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			1.5		%	26 MHz reference clock; LTE20M, 64QAM
ACLR			-48		dBc	20M offset
			-52		dBc	40M offset
Image suppression			38		dBc	Before cal
CIM3			73		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset
Transmitter 3500MHz						
Maximum output power			- 3.5		dBm	Modulation LTE 20M 64QAM
Minimum output power			-51.5		dBm	Modulation LTE 20M 64QAM
Modulation accuracy (EVM)			2		%	26 MHz reference clock; LTE20M, 64QAM
ACLR			-46		dBc	20M offset
			-55		dBc	40M offset
Image suppression			38		dBc	Before cal
CIM3			69		dBc	
CIM5			80		dBc	
CIM7			80		dBc	
RX band noise			-157		dBm/Hz	BW <=10M，30M offset
			-157		dBm/Hz	BW <=15M，45M offset
			-157		dBm/Hz	BW <=20M，55M offset

Table 11 Transmitter specifications(Low Temp)

6.3 LO Synthesizer specifications

Electrical characteristics at VDD_INTERFACE = 1.8V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Reference clock					
Reference clock (crystal oscillator or external oscillator)	12.6		122.88	MHz	
Local oscillator frequency synthesizer					
Local oscillator resolution		2.4		Hz	
Integral phase noise (10KHz~100MHz)		0.071		°rms	700MHz
		0.238		°rms	2400MHz
		0.312		°rms	3600MHz
Baseband frequency synthesizer					
Output frequency range	1800		3600	MHz	

Table 12 Frequency synthesizer indicators

6.4 Power consumption

Electrical characteristics at VDD_INTERFACE = 1.8V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
TDD TX		380		mW	N41
TDD RX		340		mW	N41
FDD TRX		550		mW	N28
Sleep mode		3		mW	No initialization required
Deep Sleep mode		0.14		mW	Need initialization

Table 13 Power consumption specifications

7. Theory of operation

7.1 General characteristics

The GC0851 is highly integrated radio frequency (RF) transceiver capable of being configured for a wide range of applications. The device integrates all RF, mixed signal, and digital blocks necessary to provide all transceiver functions in a single device. Programmability allows this broadband transceiver to be adapted for use with multiple communication standards, including frequency division duplex (FDD) and time division duplex (TDD) systems.

The GC0851 also provides self-calibration and automatic gain control (AGC) systems to maintain a high-performance level under varying temperatures and input signal conditions.

7.2 Receiver

The receiver section contains all blocks necessary to receive RF signals and convert them to analog IQ interface. There are two independently controlled channels that can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed to the signal chain, making the GC0851 suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a mixer and band shaping filter that down convert received signals to baseband for digitization. Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed.

7.3 Transmitter

The transmitter section consists of one channel that provide mixed signal, and RF blocks necessary to implement a direct conversion system.

Self-calibration circuitry is built into each transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back through an unused receiver channel to the BBP for signal monitoring. The TX monitor blocks are available only in TDD mode operation while the receiver is idle.

7.4 Clock input option

The input level of the reference clock for GC0851 ranges from 0.5Vpp to 2.5Vpp, the recommended value is 1.3Vpp. For single-ended input use case, connect a 0.1uF capacitor in series at the XTALN input, XTALP is recommended to connect to ground using a capacitor. The recommended circuit is shown as below.

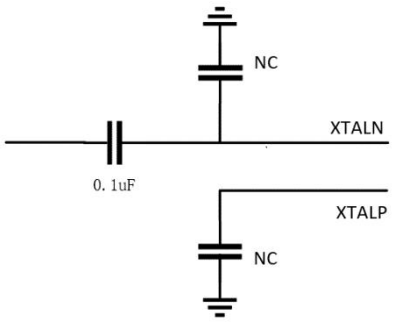

Figure 5

The reference clock can be provided by two different sources. The first option is to use a dedicated crystal with a frequency between 12.6 MHz and 122.88 MHz connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device to the XTALN pin (with the XTALP pin remaining unconnected). If an external oscillator is used, the frequency can vary between 12.6 MHz and 122.88 MHz.

This reference clock is used to supply the synthesizer blocks that generate all data clocks, sample clocks, and local oscillators inside the device. Errors in the crystal frequency can be removed by using the digitally programmable digitally controlled crystal oscillator (DCXO) function to adjust the on-chip variable capacitor. This capacitor can tune the crystal frequency variance out of the system, resulting in a more accurate reference clock from which all other frequency signals are generated. This function can also be used with on-chip temperature sensing to provide oscillator frequency temperature compensation during normal operation.

7.5 Frequency Synthesizers

RF PLLs

The GC0851 contains two identical synthesizers to generate the required LO signals for the RF signal paths: one for the receiver and one for the transmitter, and the transmitter TXLO can be shared to receivers if needed. Phase-locked loop (PLL) synthesizers are fractional-N designs incorporating completely integrated voltage controlled oscillators (VCOs) and loop filters. In TDD operation, the synthesizers turn on and off as appropriate for the RX and TX frames. In FDD mode, the TX PLL and the RX PLL can be activated simultaneously. These PLLs require no external components.

7.6 Enable state machine

The GC0851 transceiver includes an enable state machine (ENSM) that allows real-time control over the current state of the device. The device can be placed in several different states during normal operation, including

- Standby - Energy saving, frequency synthesizers disabled
- Sleep – wait with all clocks/ BB PLL disabled
- TX - The TX signal chain enabled
- RX -- The RX signal chain enabled
- FDD -- TX and RX signal chains enabled
- Alarm - Frequency synthesizers enabled

ENSM has two possible control methods: SPI control and pin control.

SPI control Mode

In SPI control mode, the ENSM is controlled asynchronously by writing SPI registers to advance the current state to the next state. The SPI control ENSM method is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for realtime control as long as the BBIC has the ability to perform timed SPI writes accurately.

Pin control mode

In pin control mode, the enable function of the ENABLE pin and the TXNRX pin allow real-time control of the current state. The ENSM allows TDD or FDD operation depending on the configuration of the corresponding SPI register. The ENABLE and TXNRX pin control method is recommended if the BBIC has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the device. To advance the current state of the ENSM to the next state, the enable function of the ENABLE pin can be driven by either a pulse (edge detected internally) or a level. When a pulse is used, it must have a minimum pulse width of one FB_CLK cycle. In level mode, the ENABLE and TXNRX pins are also edge detected by the GC0851 and must meet the same minimum pulse width requirement of one FB_CLK cycle. In FDD mode, the ENABLE and TXNRX pins can be remapped to serve as real-time RX and TX data transfer control signals. In this mode, the ENABLE pin enables or disables the receive signal path, and the TXNRX pin enables or disables the transmit signal path. In this mode, the ENSM is removed from the system for control of all data flow by these pins.

7.7 Analog IQ Interface

TX

Tx is the differential input,I+,I-,Q+,Q- respectively.Single-ended input impedance is 2.5Kohm.The common mode voltage is 0.6V.

RX

Rx is the differential output,The default common mode voltage is 0.6V(Adjustable range 0.43V~0.6V)，I or Q channel ‘s maximum output power is 10dBm.

7.8 SPI interface

The GC0851 uses a serial peripheral interface (SPI) to communicate with the BBP. This interface can only be configured as a 4-wire interface with dedicated receive and transmit ports. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol. Write commands follow a 24-bit format. The first 4 bits are used to set the bus direction and number of bytes to transfer. The next 12 bits set the address where data is to be written. The final eight bits are the data to be transferred to the specified register address (MSB to LSB). The GC0851 also supports an LSB-first format that allows the commands to be written in LSB to MSB format. In this mode, the register addresses are incremented for multibyte writes. Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DI pin and the final eight bits are read from the GC0851, which is done on the SPI_DO pin in 4-wire mode.

单位：ns

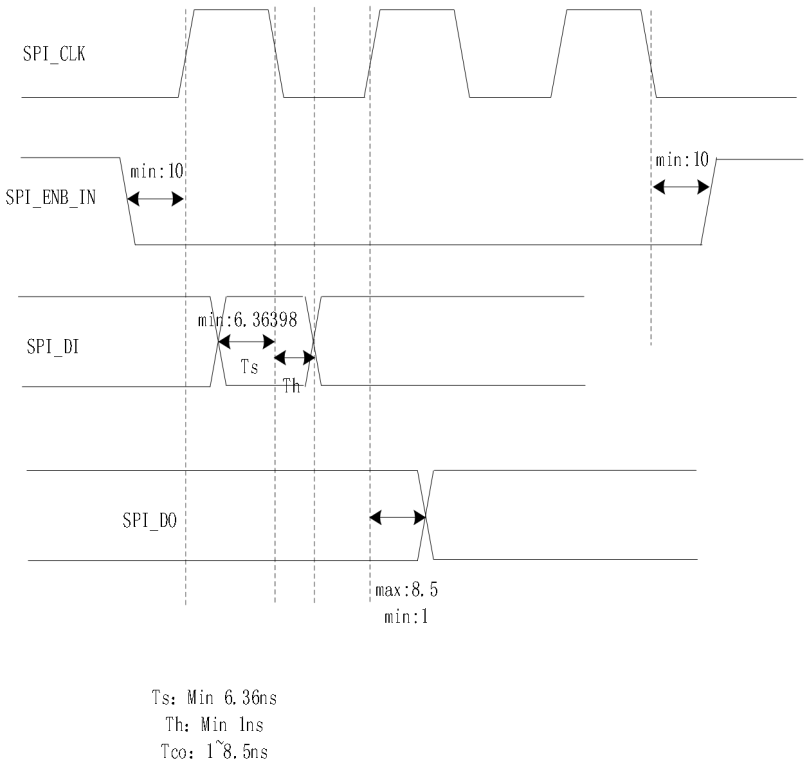

Figure 6 SPI timing

Parameter	Min	Typ	Max	Unit
High level	VDD_INTERFACE * 0.9		VDD_INTERFACE	V
Low level	0		VDD_INTERFACE * 0.1	V
SPI_CLK period		40		ns
SPI_CLK pulse width	25			ns
SPI_CLK Rising transition	0		4	ns
SPI_CLK Rising transition	0		4	ns
SPI_ENB setup to first SPI_CLK rising edge	10			ns
Last SPI_CLK falling edge to SPI_ENB hold	10			ns

Table 14 SPI timing specifications

7.9 General control pins

Control outputs (CTRL_OUT[7:0])

GC0851 provides eight simultaneous real-time output signals for use as interrupts to the BBP. These outputs can be configured to output a number of internal settings and measurements that the BBP can use when monitoring transceiver performance in different situations. The control output pointer register selects what information is output to these pins, and the control output enable register determines which signals are activated for monitoring by the BBP. Signals used for manual gain mode, calibration flags, state machine states, and the ADC output are among the outputs that can be monitored on these pins.

Control input (CTRL_IN[3:0])

GC0851 provides four edge detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of the pins to change the transmit gain in real time.

7.10 Auxiliary converter AUXADC

The GC0851 contains two auxiliary ADCs that can be used to monitor system functions such as temperature or power output. The converter is 12 bits wide and has an input range of 0 V to 1 V. When enabled, the ADC is in a free running state. SPI reads provide the last value latched at the ADC output. A multiplexer in front of the ADC allows the user to select between the AUXADC input pin and a built-in temperature sensor. AUXADC cannot be occupied during initialization, calibration and RX peak detection.

7.11 GC0851 power supply

The GC0851 must be powered by the following two supplies: the analog supply (VDDD1P3_DIG/VDDAx = 1.3 V), the interface supply (VDD_INTERFACE = 2.5V or 1.8V or 3.3V). For applications requiring optimal noise performance, it is recommended that the 1.3 V supply be sourced from low noise, low dropout (LDO) regulators.

For applications that optimal noise performance is not critical but board space is important, the 1.3V power rail can be supplied directly from a switch and an integrated power management unit (PMU) can be adopted.

8. Revision history

Editions	Dates	Description
0.1	2024/11	Draft
1.0	2025/03	First release to customer
1.1	2025/8/11	Update 5.1 Outline dimensions
1.2	2025/11/17	Update Outline dimensions

9. Ordering information

Model	Package	Packaging Form	Minimum Order Quantity
GC0851	BGA82 4.5*5 mm	REEL	3000

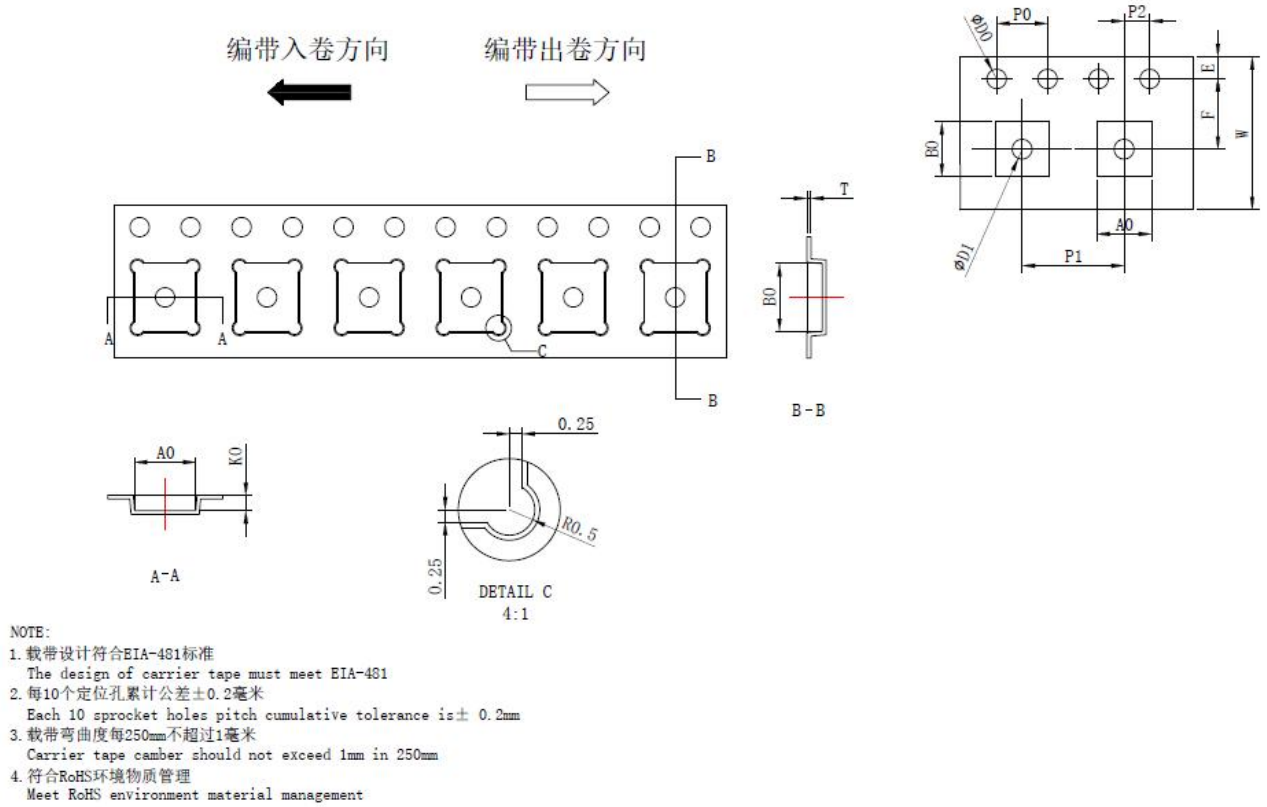

Figure7 Packaging information

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