1.FEATURES

- 2T2R Mixer
- Integrated PLL
- SPI Read/Write
- 500MHz~5000MHz LO Frequency Range
- 30MHz to 7100MHz Mixer Frequency Range
- 19.2,20,26,30.72,38.4,52MHz External Reference Oscillator
- Up to 100MHz Bandwidth
- Programmable Conversion Gain
- LO Lock Detection
- Low Current Consumption
- 4-Wire Serial Interface
- Market Proven CMOS Technology
- QFN 24 (3x3x0.85 mm) Package

2.APPLICATIONS

- General-purpose radio systems
- Femtocell/picocell/microcell base stations
- Multifunctional intelligent terminal
- Point to point communication systems
- Wideband Radios
- Frequency Band Shifters
- WiMax/LTE Infrastructure
- Distributed Antenna Systems

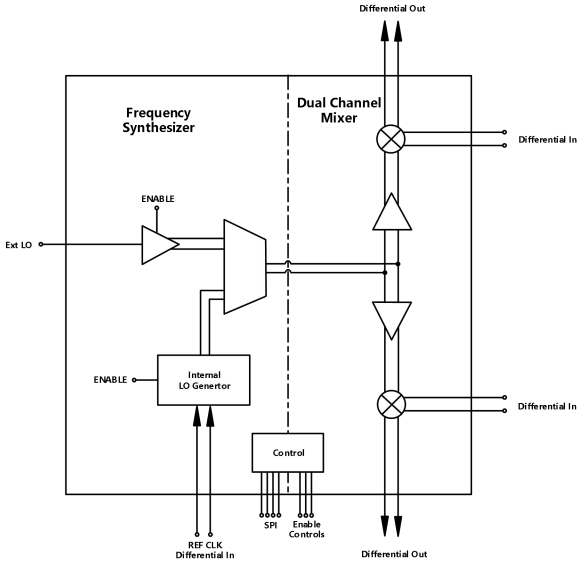

Figure 1. Block Diagram

3.GENERAL DESCRIPTION

The GC0861 is a high performance, highly integrated ultra-wideband 2T2R mixer with PLL. The fractional-N synthesizer takes advantage of an advanced sigma-delta modulator that delivers ultra-fine step sizes and low spurious products. GC0861 can up/down-convert frequencies ranging from 30 MHz to 7100 MHz. RF input and IF output are all differential. Device programming is achieved via a simple 4-wire serial interface.The mixer support 5G New Radio(NR) in FR-1 , sub 6GHz band.

The chip is housed in a compact 3 mm × 3 mm QFN package. Integrated PLL with loop filter helps minizing the PCB size when in custom design.

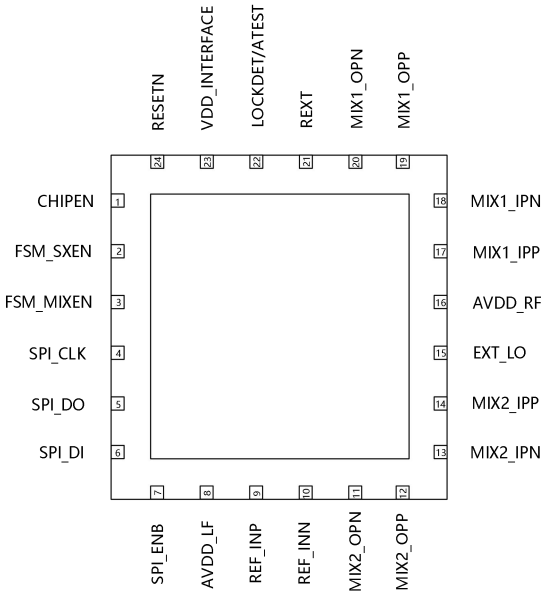

Figure 2. Pinout (Top View)

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4. Absolute Maximum Ratings

Parameter	Range	Unit	Condition
Supply Voltage AVDD_LF	2	V	
Supply Voltage AVDD_RF	2	V	
Supply Voltage VDD_INTERFACE	3.6	V	
Maximum input power	15	dBm	RMS power
ESD (HBM)	±4000	V	
ESD (CDM)	±300	V	
Junction Temperature	+125	°C	

Table 1

5. Pin Description

Name	Pin	Description
CHIPEN	1	CHIP Enable pin（Control Logic）
FSM_SXEN	2	FSM Synthesizer Enable（Control Logic）
FSM_MIXEN	3	FSM Mixer Enable（Control Logic）
SPI_CLK	4	Serial interface clock
SPI_DO	5	Serial interface data out
SPI_DI	6	Serial interface data in
SPI_ENB	7	Serial interface Chip Select (active low)
AVDD_LF	8	Analog Supply for Low Frequency blocks (default 1.3V)
REF_INP	9	Reference input P. Use AC coupling capacitor
REF_INN	10	Reference input N. Use AC coupling capacitor(This pin can be used as a single ended input through coupling capacitor,The REF_INP pin needs to be grounded through a capacitor)
MIX2_OPN	11	Differential output 2
MIX2_OPP	12	Differential output 2
MIX2_IPN	13	Differential input 2
MIX2_IPP	14	Differential input 2
EXT_LO	15	Not connect
AVDD_RF	16	Analog Supply RF (default 1.3V)
MIX1_IPP	17	Differential input 1
MIX1_IPN	18	Differential input 1
MIX1_OPP	19	Differential output 1
MIX1_OPN	20	Differential output 1
REXT	21	External bandgap bias resistor
LOCKDET/ATEST	22	Lock detect output / Analog Test pin
VDD_INTERFACE	23	VDD Interface (default 2.5V)
RESETX	24	Chip reset (active low). Connect to DIG_VDD if asynchronous reset is not required.

Table 2

ESD HANDLING: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.

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6. Recommended Operating Condition

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
AVDD_LF	1.15	1.3	1.5	V	
AVDD_RF	1.15	1.3	1.5	V	
VDD_INTERFACE	1.8	2.5	3.3	V	
Control Logic High		VDD_INTERFACE		V	
Control Logic Low		0	0.3	V	
Operating Temperature	-40	25	+85	°C	
Storage Temperature	-55	25	+150	°C	

Table 3

7. Serial Peripheral Interface (SPI)

The GC0861 SPI is a flexible, synchronous serial communications bus allowing seamless interfacing to many industry standard microcontrollers and microprocessors. The GC0861 cannot be used to control other devices on the bus – it only operates as a slave.

There are two phases to a communication cycle. Phase 1 is the control cycle, which is the writing of a control word into the GC0861. The control word provides the GC0861 serial port controller with information regarding the data field transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 control field defines whether the upcoming data transfer is read or write. It also defines the register address being accessed.

Phase 1 Instruction Format

The 16-bit control field contains the following information:

MSB	D14	D13	D12	D11:D0
W/Rb	NB2	NB1	NB0	A<11:0>

Table 4

W/Rb — Bit 15 of the instruction word determines whether a read or write data transfer occurs after the instruction byte write. Logic high indicates a write operation; logic zero indicates a read operation.

D11:D0 – Bits <11:0> specify the starting byte address for the data transfer during Phase 2 of the IO operation.

All byte addresses, both starting and internally generated addresses, are assumed to be valid. That is, if an invalid address (undefined register) is accessed, the IO operation continues as if the address space were valid. For write operations, the written bits are discarded, and read operations result in logic zeros at the output.

Single-Byte Data Transfer

When NB2, NB1, and NB0 are all zero, a single-byte data transfer is selected. In this scenario, the next eight bits to follow the address bits contain the data being written to or read from the GC0861 register. Once the final bit is transferred, the data signals return to their idle states and the SPI_ENB signal goes high to end the communication session.

The following diagrams in Figure 3 and Figure 4 detail the SPI bus waveforms for a single-register write operation and a single-register read operation, respectively. In the first figure, the value 0x55 is written to register 0x15A. In the second value, register 0x15A is read and the value returned by the device is 0x55.

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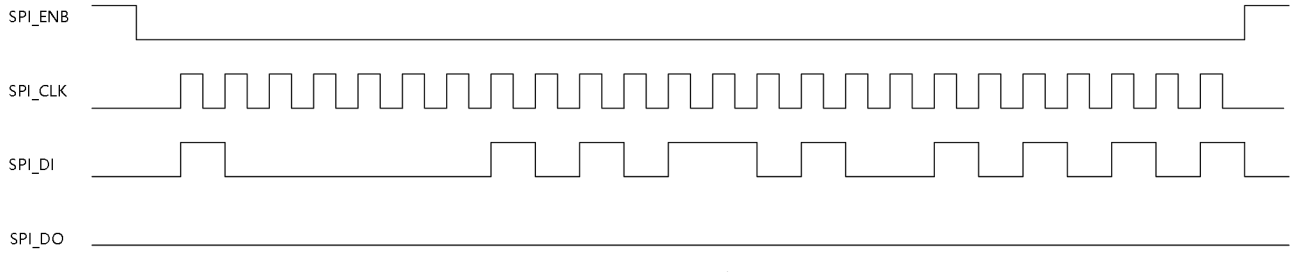

Figure 3. Nominal Timing Diagram, SPI Write

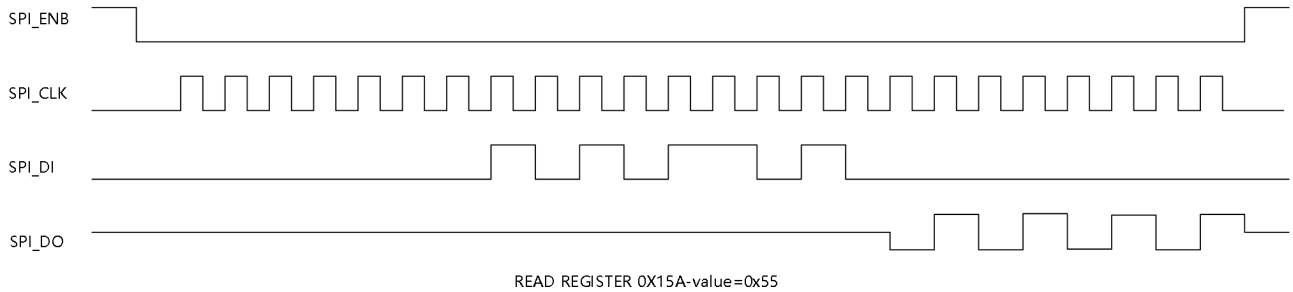

Figure 4. Nominal Timing Diagram, SPI Read

Table 5 lists the timing specifications for the SPI bus. The relationship between these parameters is shown in Figure 5.

Parameter	Min	Typical	Max	Description
tCP		48ns		SPI_CLK cycle time (clock period)
tMP		25ns		SPI_CLK pulse width
tSC		25ns		SPI_ENB setup time to first SPI_CLK rising edge
tHC		25ns		Last SPI_CLK falling edge to SPI_ENB hold
tS		23ns		SPI_DI data input setup time to SPI_CLK
tH		25ns		SPI_DI data input hold time to SPI_CLK
tCO		3ns		SPI_CLK rising edge to output data delay (4-wire mode)
tHZM		46ns		Bus turnaround time after BBP drives the last address bit
tHZS		3ns		Bus turnaround time after GC0861 drives the last data bit

Table 5. SPI Bus Timing Constraint Values

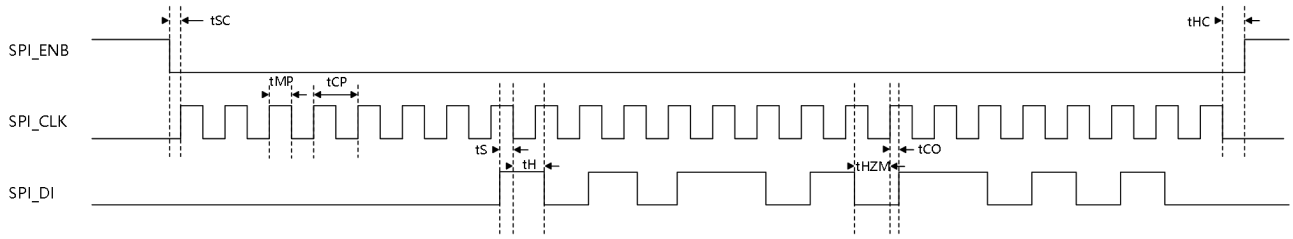

Figure 5. SPI Timing with Parameter Labels

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8. Electrical Specifications

Here are the performance indicators for three application cases, with other cases depending on the actual situation of the customer.

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,800MHz Downconverted To 300MHz,Reference Clock input REF-INN pin;The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun:HHM1591A2(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1591a2_en.pdf), OutputBalun:HHM1591D1(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1591d1_en.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	800	-	MHz	
IF Frequency	-	300	-	MHz	
LO Frequency	-	500	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	3.5	4	4.5	dB	
OP1	-1.5	-0.5		dBm	
OIP3	13	15		dBm	
ACLR		-56	-53	dBc	RF:LTE FDD DL 20M 64QAM;Power:-12dBm
EVM		0.4	0.5	%	RF:LTE FDD DL 20M 64QAM;Power:-12dBm
NF		8.5	9.5	dB	
Phase Noise @LO		0.09		deg	1K~20MHz
2nd LO Harmonic Suppression		-76		dBm	Test with Balun
3rd LO Harmonic Suppression		-90		dBm	Test with Balun
LO-IF amplitude		-52		dBm	Test with Balun(Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		120	140	mW	MIX1&MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 6

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,300MHz Upconverted To 800MHz,Reference Clock input REF-INN pin,The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun: HHM1591D1(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1591d1_en.pdf),OutputBalun:HHM1591A2(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1591a2_en.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	300	-	MHz	
IF Frequency	-	800	-	MHz	
LO Frequency	-	500	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	1	1.5	2	dB	
OP1	-0.5	0		dBm	
OIP3	14.5	15.5		dBm	
ACLR		-57	-56	dBc	RF:LTE FDD DL 20M 64QAM;Power:-12dBm

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EVM		0.45	0.5	%	RF:LTE FDD DL 20M 64QAM;Power:-12dBm
NF		5.5	8	dB	
Phase Noise @LO		0.09		deg	1K~20MHz
2nd LO Harmonic Suppression		-60		dBm	Test with Balun
3rd LO Harmonic Suppression		-69		dBm	Test with Balun
LO-IF amplitude		-46		dBm	Test with Balun(Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		105	120	mW	MIX1&MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 7

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,5725MHz Downconverted To 3600MHz,Reference Clock input REF-INN pin,The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun:HHM1908A2(https://product.tdk.com.cn/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1908a2_zh.pdf),OutputBalun:HHM1711Q1(https://product.tdk.com.cn/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1711q1_zh.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	5725	-	MHz	
IF Frequency	-	3600	-	MHz	
LO Frequency	-	2125	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	-1	0	0.5	dB	
IF output flatness		2		dB	100MHz Bandwidth;Depending on the matching network
OP1	1	1.5		dBm	
OIP3	13.5	15.5		dBm	
ACLR		-53	-50	dBc	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
EVM		0.9	1.1	%	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
NF		6.5	7.5	dB	
Phase Noise @LO		0.4		deg	1K~20MHz
2nd LO Harmonic Suppression		-62		dBm	Test with Balun
3rd LO Harmonic Suppression		-96		dBm	Test with Balun
LO-IF amplitude		-53		dBm	Test with Balun (Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		125	145	mW	MIX1&MIX2 on
Power Consumption		95	115	mW	MIX1 or MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 8

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,3600MHz Upconverted To 5725MHz,Reference

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Clock input REF-INN pin,The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun:HHM1711Q1(https://product.tdk.com.cn/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1711q1_zh.pdf),OutputBalun:HHM1908A2(https://product.tdk.com.cn/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1908a2_zh.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	3600	-	MHz	
IF Frequency	-	5725	-	MHz	
LO Frequency	-	2125	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	-6	-5.5	-5	dB	
IF output flatness		1.5		dB	100MHz Bandwidth;Depending on the matching network
OP1	-1.5	-0.5		dBm	
OIP3	9.5	11.5		dBm	
ACLR		-53	-50	dBc	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
EVM		1.1	1.3	%	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
NF		9.3	10	dB	
Phase Noise @LO		0.4		deg	1K~20MHz
2nd LO Harmonic Suppression		-53		dBm	Test with Balun
3rd LO Harmonic Suppression		-65		dBm	Test with Balun
LO-IF amplitude		-52		dBm	Test with Balun (Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		125	145	mW	MIX1&MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 9

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,7100MHz Downconverted To 2100MHz,Reference Clock input REF-INN pin,The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun: HHM1595A1(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1595a1_en.pdf),Output Balun: HHM1927A4 (https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1927a4_en.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	7100	-	MHz	
IF Frequency	-	2100	-	MHz	
LO Frequency	-	5000	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	-0.5	0.5	1	dB	
IF output flatness		1		dB	100MHz Bandwidth;Depending on the matching network
OP1	3.5	4		dBm	
OIP3	15	16.5		dBm	
ACLR		-52	-50	dBc	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
EVM		1.8	2	%	RF:5GNR FDD DL100M 256QAM;Power:-12dBm

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NF		7	8	dB	
Phase Noise @LO		0.6		deg	1K~20MHz
2nd LO Harmonic Suppression		-40		dBm	Test with Balun
3rd LO Harmonic Suppression		-64		dBm	Test with Balun
LO-IF amplitude		-79		dBm	Test with Balun (Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		140	160	mW	MIX1&MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 10

AVDD_LF=1.3V,AVDD_RF=1.3V,VDD_INTERFACE=2.5V,Temp=25°C,2100MHz Upconverted To 7100MHz,Reference Clock input REF-INN pin,The Attenuation Is Set To 0,The Data Represents The Two Channels Of The Mixer,Input Balun: HHM1927A4(https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1927a4_en.pdf),Output Balun: HHM1595A1 (https://product.tdk.com/system/files/dam/doc/product/rf/rf/balun/catalog/rf_balun_hhm1595a1_en.pdf).

Parameter	Min	Typ	Max	Unit	Condition
RF Frequency	-	2100	-	MHz	
IF Frequency	-	7100	-	MHz	
LO Frequency	-	5000	-	MHz	
External Reference Oscillator	-	30.72	-	MHz	
Gain	-9.5	-7.5	-6.5	dB	
IF output flatness		0.8		dB	100MHz Bandwidth;Depending on the matching network
OP1	-2	0.5		dBm	
OIP3	8	11		dBm	
ACLR		-52	-50	dBc	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
EVM		1.8	2.1	%	RF:5GNR FDD DL100M 256QAM;Power:-12dBm
NF		10.5	12	dB	
Phase Noise @LO		0.6		deg	1K~20MHz
2nd LO Harmonic Suppression		-51		dBm	Test with Balun
3rd LO Harmonic Suppression		-83		dBm	Test with Balun
LO-IF amplitude		-57		dBm	Test with Balun(Adjusting registers to achieve optimal performance)
S11		-10		dB	Include IF,RF Port; Test with Balun
Power Consumption		135	150	mW	MIX1&MIX2 on
Power Consumption		10		uW	CHIPEN=0
LO step size		8		Hz	
LO Lock time		25		us	

Table 11

9. Evaluation Board Schematic & Bill of Materials

NOTE:Here are the application schematics and bill of materials of three application cases for reference;The matching network needs to be adjusted due to the different actual applications of customers; Select the appropriate balun

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based on the operating frequency of RF and IF;Tuning the RF and IF matching network according to their operating frequency.;The impedance of RF single-end is 50Ω,and the impedance of differential is 100Ω.

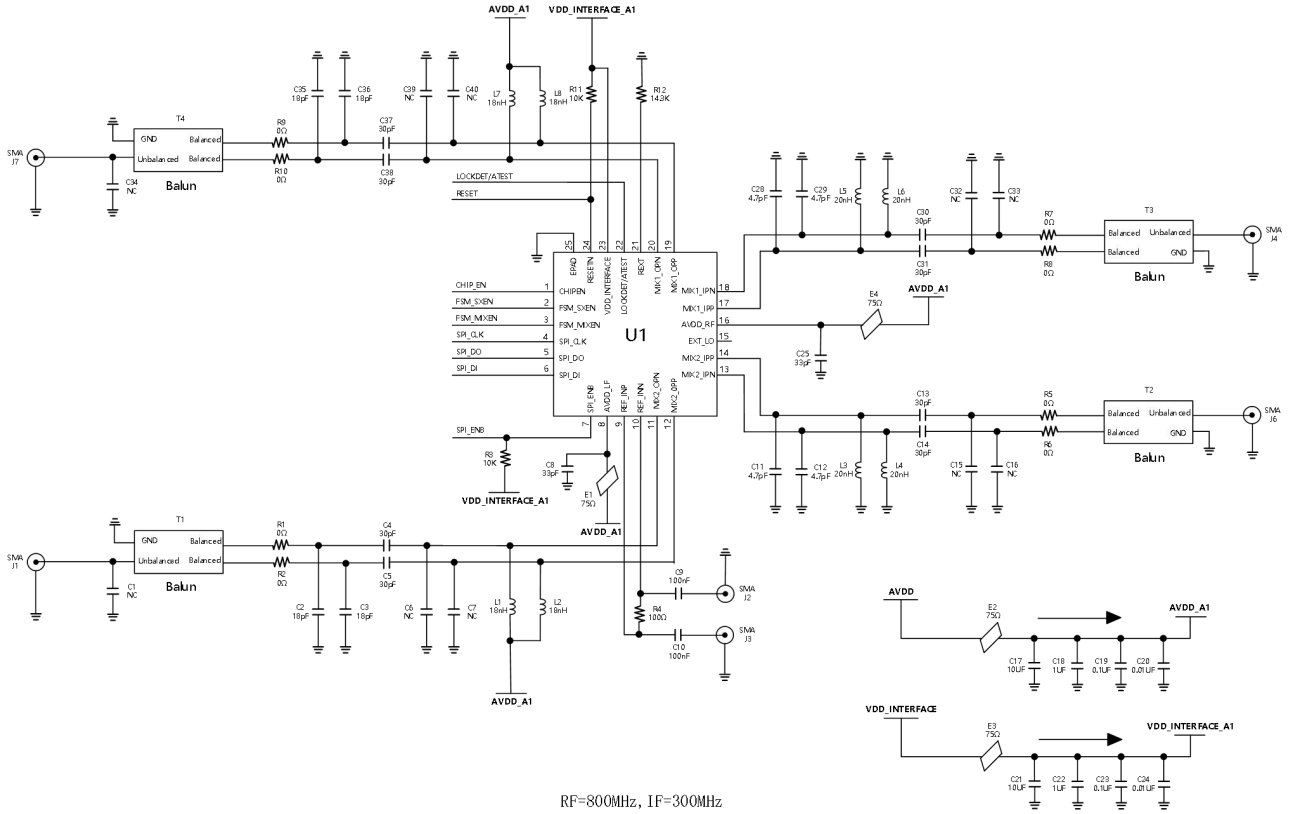

Figure 6. Evaluation Board Schematic for 800MHz to 300MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C2,C3,C35,C36,	18pF	muRata	GRM0335C1H180JA01D	0201	18pF,50V
C4,C5,C13,C14,C30,C31,C37,C38,	30pF	muRata	GRM0335C1H300JA01D	0201	30pF,50V
C8,C25	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C9,C10,C19,C23	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C11,C12,C28,C29	4.7pF	muRata	GRM0335C1H4R7CA01D	0201	4.7pF,50V
C17,C21	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C18,C22	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C20,C24	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
R1,R2,R5,R6,R7,R8,R9,R10	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R3,R11	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R4	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R12	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L7,L8	18nH	muRata	LQP03HQ18NJ02D	0201	0201,18nH
L3,L4,L5,L6	20nH	muRata	LQP03HQ20NH02D	0201	0201,20nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads
T1,T4	Balun	TDK	HHM1591D1	0805	350-470MHz Balun
T2,T3	Balun	TDK	HHM1591A2	0805	350-950MHz Balun
J1,J2,J3,J4,J6,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch

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C1,C34	NC			0402	
C6,C7,C15,C16,C32,C33,C39,C40	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 12. Evaluation Board Bill of Materials for 800MHz to 300MHz Application

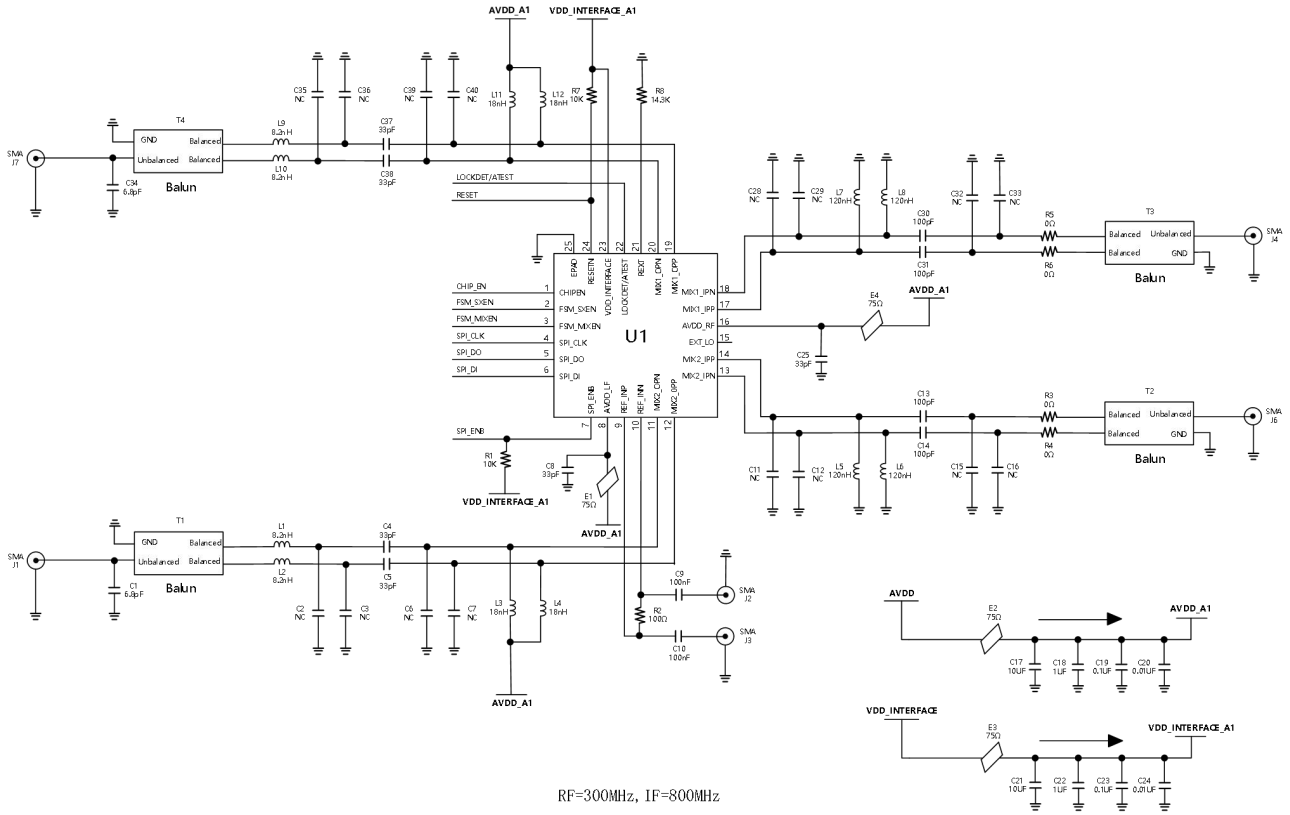

Figure 7. Evaluation Board Schematic for 300MHz to 800MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C1,C34,	6.8pF	muRata	GRM1555C1H6R8BA01D	0402	6.8pF,50V
C4,C5,C8,C25,C37,C38	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C9,C10,C19,C23	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C13,C14,C30,C31	100pF	muRata	GRM0335C1H101JA01D	0201	100pF,50V
C17,C21	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C18,C22	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C20,C24	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
R1,R7	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R2	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R3,R4,R5,R6	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R8	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L9,L10	8.2nH	muRata	LQP03HQ8N2H02D	0201	0201,8.2nH
L3,L4,L11,L12	18nH	muRata	LQP03HQ18NJ02D	0201	0201,18nH
L5,L6,L7,L8	120nH	muRata	LQP03HQR12J02D	0201	0201,120nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads
T1,T4	Balun	TDK	HHM1591A2	0805	350-950MHz Balun
T2,T3	Balun	TDK	HHM1591D1	0805	350-470MHz Balun
J1,J2,J3,J4,J6,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch

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C2,C3,C6,C7,C11,C12,C15,C16,C28,C29,C32,C33,C35,C36,C39,C40	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 13. Evaluation Board Bill of Materials for 300MHz to 800MHz Application

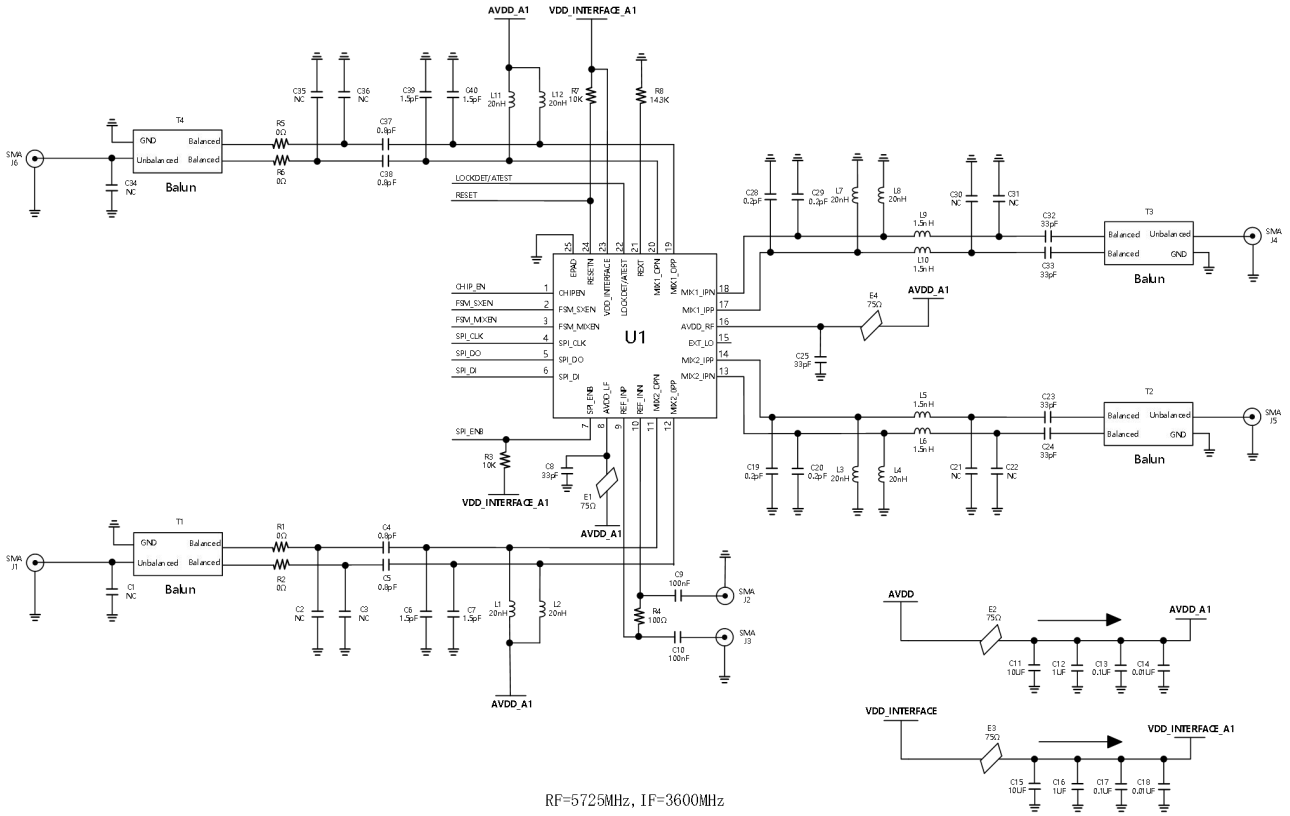

Figure 8. Evaluation Board Schematic for 5725MHz to 3600MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C4,C5,C37,C38	0.8pF	muRata	GRM0335C1HR80BA01D	0201	0.8pF,50V
C6,C7,C39,C40	1.5pF	muRata	GRM0335C1H1R5CA01D	0201	1.5pF,50V
C8,C23,C24,C25,C32,C33	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C9,C10,C13,C17	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C11,C15	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C12,C16	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C14,C18	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
C19,C20,C28,C29	0.2pF	muRata	GRM0335C1HR20BA01D	0201	0.2pF,50V
R1,R2,R5,R6	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R3,R7	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R4	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R8	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L3,L4,L7,L8,L11,L12	20nH	muRata	LQP03HQ20NH02D	0201	0201,20nH
L5,L6,L9,L10	1.5nH	muRata	LQP03HQ1N5B02D	0201	0201,1.5nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads
T1,T4	Balun	TDK	HHM1711Q1	0603	2300-3800MHz Balun
T2,T3	Balun	TDK	HHM1908A2	0402	4900-5950MHz Balun

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J1,J2,J3,J4,J5,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch
C1,C34	NC			0402	
C2,C3,C21,C22,C30,C31,C35,C36	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 14. Evaluation Board Bill of Materials for 5725MHz to 3600MHz Application

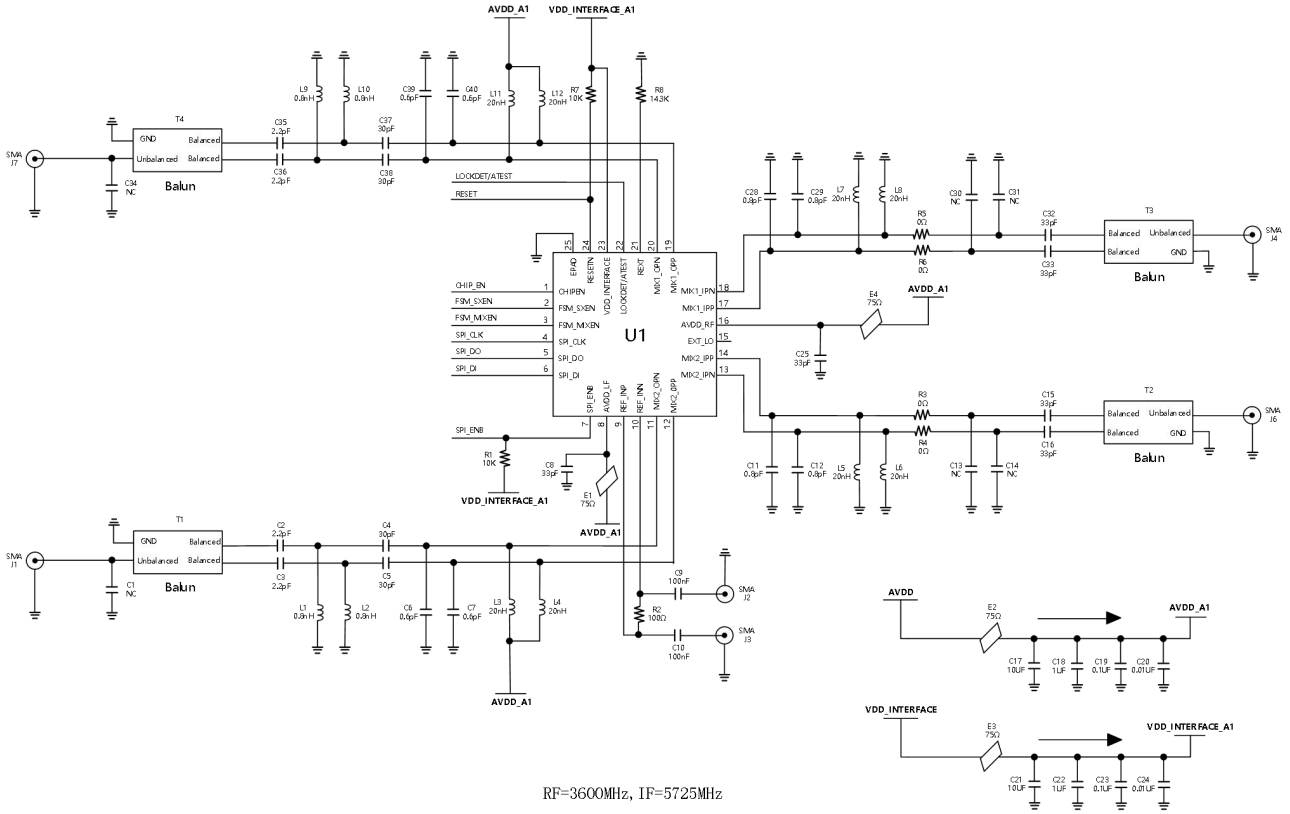

Figure 9. Evaluation Board Schematic for 3600MHz to 5725MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C2,C3,C35,C36	2.2pF	muRata	GRM0335C1H2R2CA01D	0201	2.2pF,50V
C4,C5,C37,C38	30pF	muRata	GRM0335C1H300JA01D	0201	30pF,50V
C6,C7,C39,C40	0.6pF	muRata	GRM0335C1HR60BA01D	0201	0.6pF,50V
C8,C15,C16,C25,C32,C33	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C9,C10,C19,C23	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C11,C12,C28,C29	0.8pF	muRata	GRM0335C1HR80BA01D	0201	0.8pF,50V
C17,C21	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C18,C22	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C20,C24	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
R1,R7	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R2	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R3,R4,R5,R6	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R8	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L9,L10	0.8nH	muRata	LQP03TN0N8B00D	0201	0201,0.8nH
L3,L4,L5,L6,L7,L8,L11,L12	20nH	muRata	LQP03HQ20NH02D	0201	0201,20nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads

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T1,T4	Balun	TDK	HHM1908A2	0402	4900-5950MHz Balun
T2,T3	Balun	TDK	HHM1711Q1	0603	2300-3800MHz Balun
J1,J2,J3,J4,J6,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch
C1,C34	NC			0402	
C13,C14,C30,C31	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 15. Evaluation Board Bill of Materials for 3600MHz to 5725MHz Application

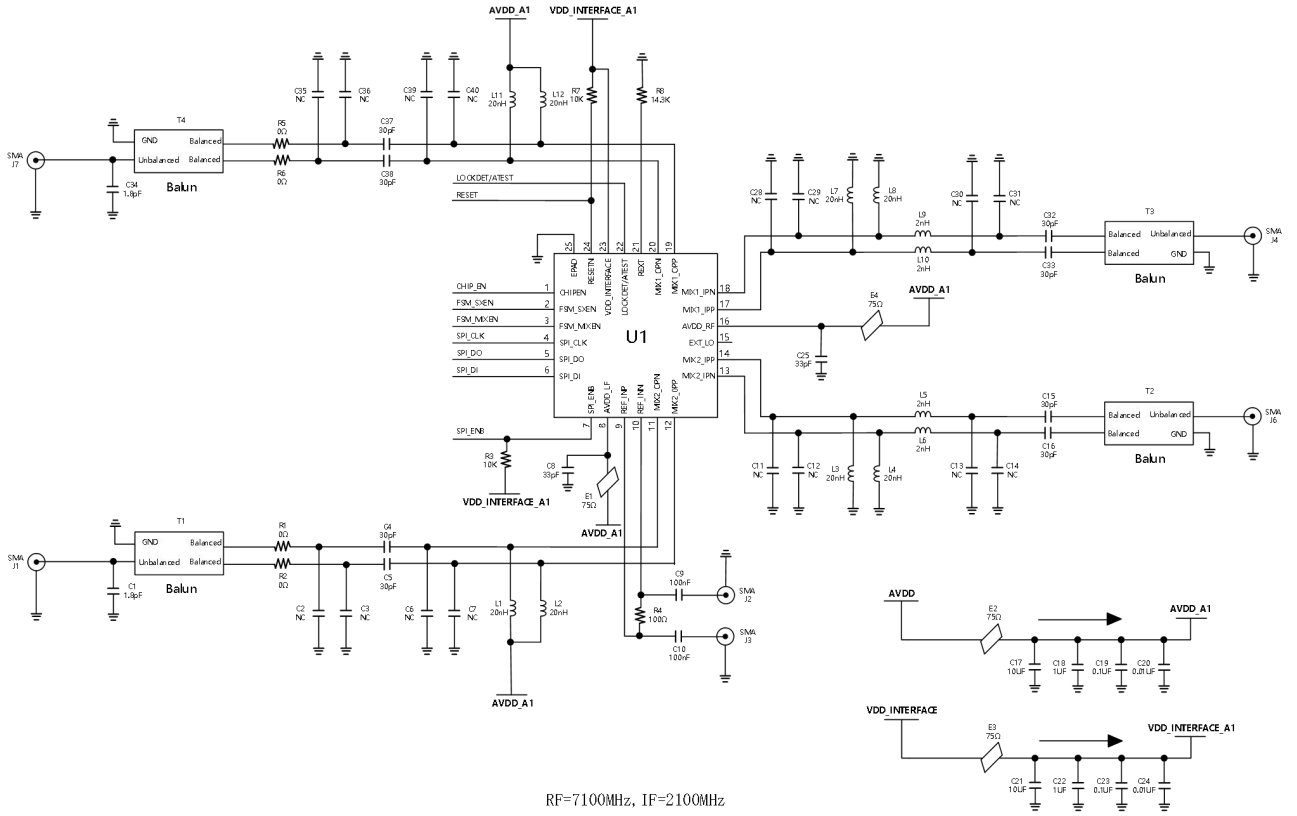

Figure 10. Evaluation Board Schematic for 7100MHz to 2100MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C1,C34	1.8pF	muRata	GRM1555C1H1R8BA01D	0402	1.8pF,50V
C4,C5,C15,C16,C32,C33,C37,C38	30pF	muRata	GRM0335C1H300JA01D	0201	30pF,50V
C8,C25	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C9,C10,C19,C23	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C17,C21	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C18,C22	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C20,C24	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
R1,R2,R5,R6	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R3,R7	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R4,	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R8	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L3,L4,L7,L8,L11,L12	20nH	muRata	LQP03HQ20NH02D	0201	0201,20nH
L5,L6,L9,L10	2nH	muRata	LQP03HQ2N0B02D	0201	0201,2nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads
T1,T4	Balun	TDK	HHM1927A4	0402	1805-2170MHz Balun

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T2,T3	Balun	TDK	HHM1595A1	0805	3000-8000MHz Balun
J1,J2,J3,J4,J6,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch
C2,C3,C6,C7,C11,C12,C13,C14,C28,C29, C30,C31,C35,C36,C39,C40	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 16. Evaluation Board Bill of Materials for 7100MHz to 2100MHz Application

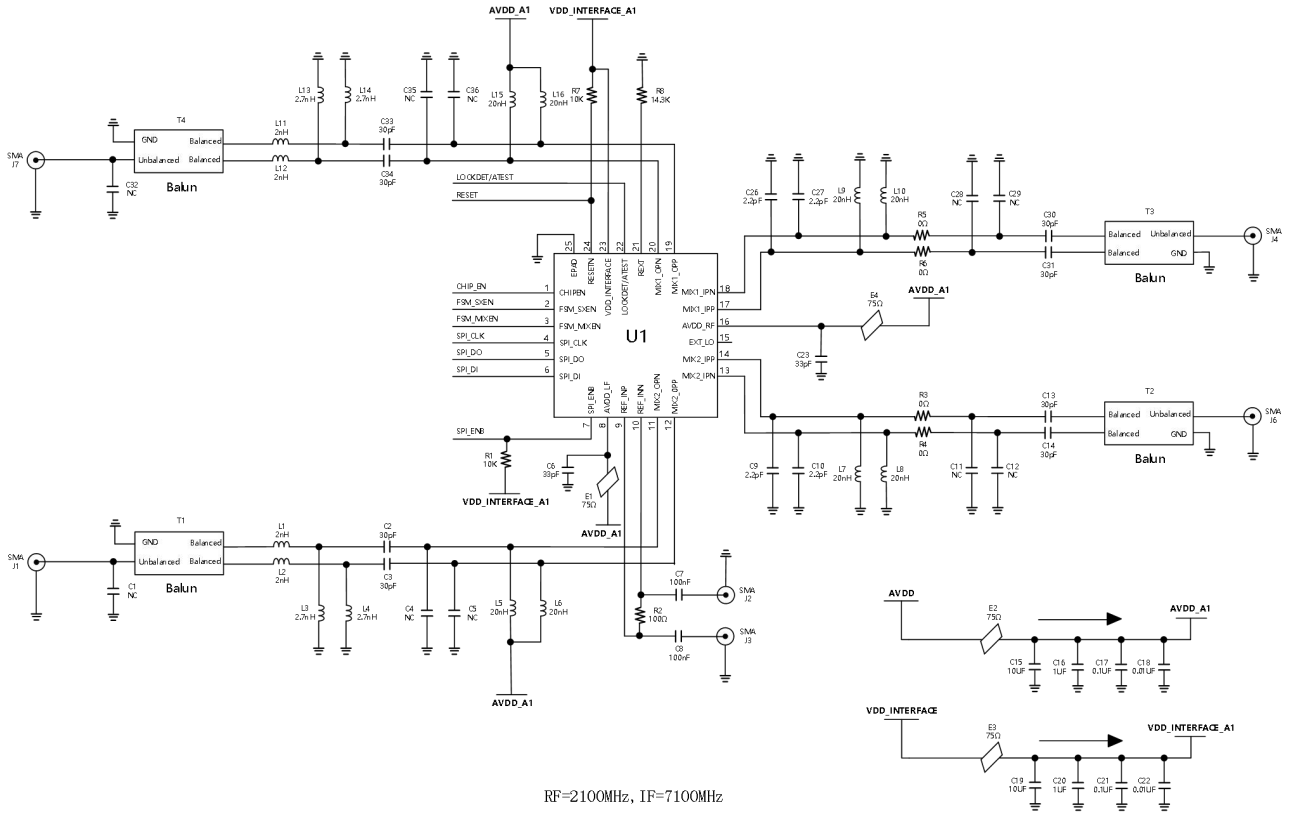

Figure 11. Evaluation Board Schematic for 2100MHz to 7100MHz Application

Component	Value	Manufacturer	Mfr Part Number	Size	Description
C2,C3,C13,C14,C30,C31,C33,C34	30pF	muRata	GRM0335C1H300JA01D	0201	30pF,50V
C6,C23	33pF	muRata	GRM0335C1H330JA01D	0201	33pF,50V
C7,C8,C17,C21	100nF	muRata	GCM033R71A103KA3D	0201	100nF,±10%,10V
C9,C10,C26,C27	2.2pF	muRata	GRM0335C1H2R2CA01D	0201	2.2pF,50V
C15,C19	10uF	Fenghua	0603X106K6R3NT	0603	10uF,±10%
C16,C20	1uF	Taiyo	JMK105BJ105MV8F	0402	1uF,20%,6.3V
C18,C22	10nF	YAGEO	CC0201KRX5R5BB103	0201	10nF,±10%,6.3V
R1,R7	10kΩ	YAGEO	RC0201JR-0710KL	0201	10kΩ,±5%,50mW
R2	100Ω	YAGEO	RC0201JR-07100RL	0201	100Ω,±5%,50mW
R3,R4,R5,R6	0Ω	YAGEO	RC0201JR-070RL	0201	0Ω,±5%,50mW
R8	14.3kΩ	Fenghua	RC-01W1432FT	0201	14.3kΩ,±1%,1/20W
L1,L2,L11,L12	2nH	muRata	LQP03HQ2N0B02D	0201	0201,2nH
L3,L4,L13,L14	2.7nH	muRata	LQP03HQ2N7B02D	0201	0201,2.7nH
L5,L6,L7,L8,L9,L10,L15,L16	20nH	muRata	LQP03HQ20NH02D	0201	0201,20nH
E1,E2,E3,E4	75Ω	muRata	BLM15BA750SN1D	0402	75Ω,25%,Ferrite Beads
T1,T4	Balun	TDK	HHM1595A1	0805	3000-8000MHz Balun

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T2,T3	Balun	TDK	HHM1927A4	0402	1805-2170MHz Balun
J1,J2,J3,J4,J6,J7	SMA	Johnson	142-0701-851	end launch	SMA end launch
C1,C32	NC			0402	
C4,C5,C11,C12,C28,C29,C35,C36	NC			0201	
U1	GC0861	Geochip	GC0861	QFN 24-Pin 3X3	30 to 7100MHz Mixer

Table 17. Evaluation Board Bill of Materials for 2100MHz to 7100MHz Application

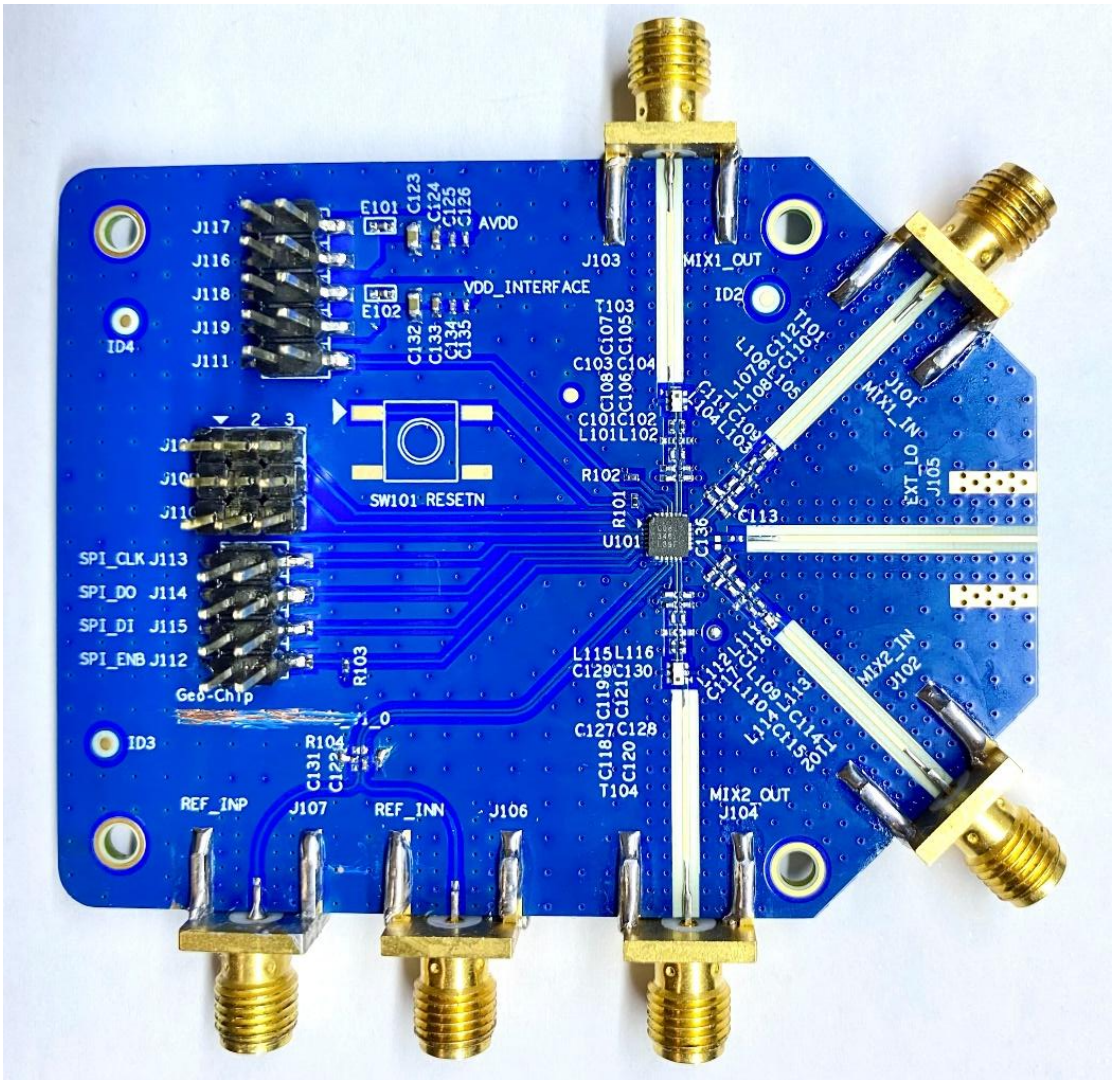

Figure 12. Actual images of the Evaluation Board

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10. Package Dimensions

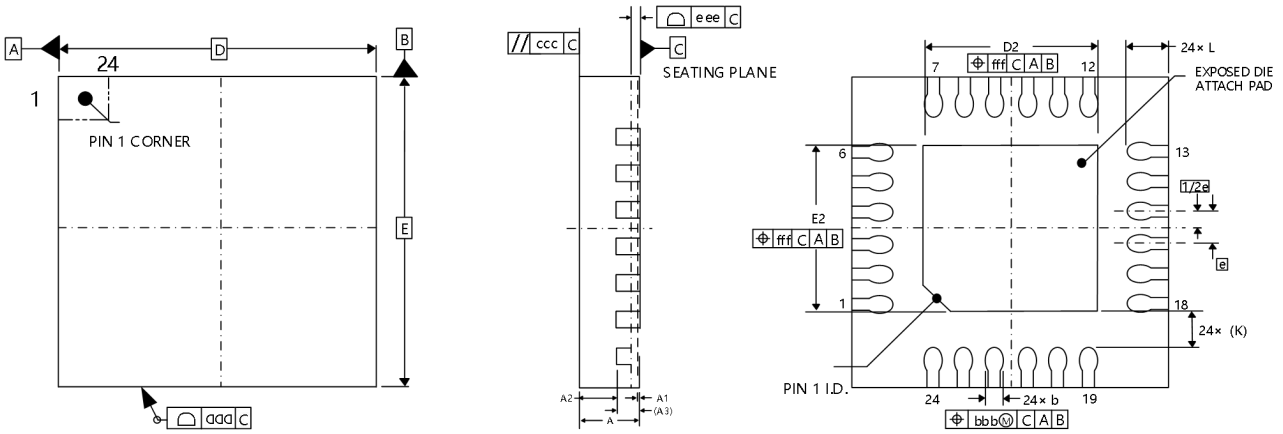

Figure 13. Package View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.12	0.17	0.22
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	1.8	1.9	2
	Y	E2	1.8	1.9	2
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Table 18. 24-Pin QFN Package Dimensions (unit mm)

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11. Part Marking

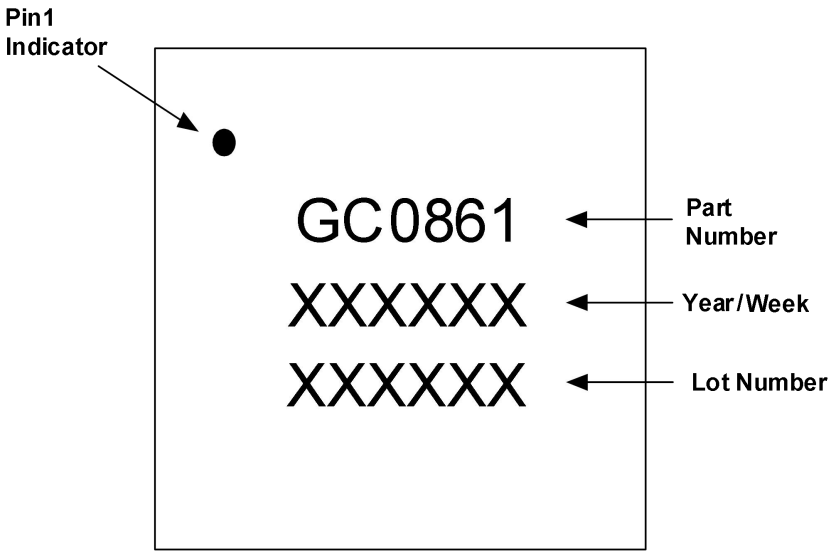

Figure 14. Typical Part Markings (Top View)

12. Packaging Information

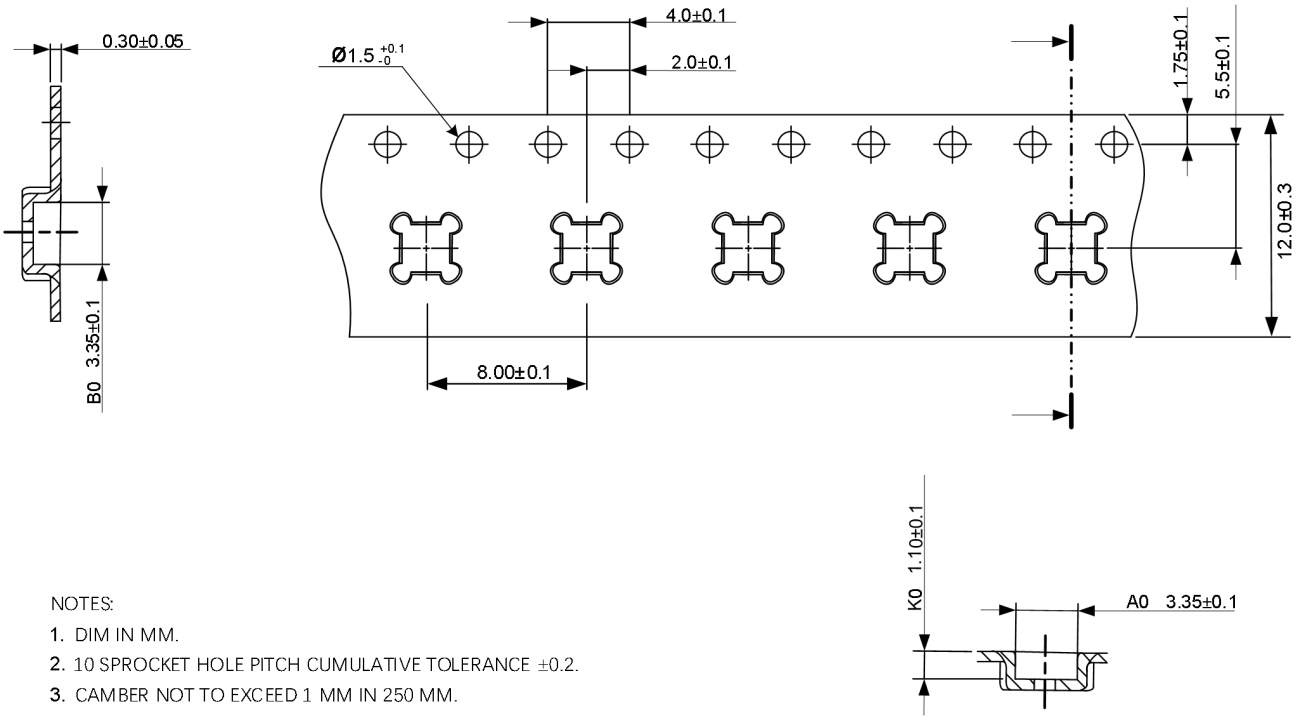

Figure 15. Packaging Information

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China Tel: + 86-571 26283530

14. Ordering Information

Model	Encapsulation	Packaging Form	Minimum Order Quantity
GC0861	QFN3*3-0.85	Tape and Reel	3000

15. Revision Record

Version	Date	Description
1.0	5/9/2024	Initial version
1.1	8/14/2024	Modify the EXT_LO Pin description,Schematic and BOM
1.2	8/14/2025	Add single mixer channel Power Consumption

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